

## CLAIMS

What is claimed is:

- 1           1.     An image signal processor comprising:  
2           a local memory to store data; and  
3           a memory command handler including a plurality of memory address  
4     generators, each memory address generator to generate a memory address to the local  
5     memory and to interpret a command to be performed on the data of the local memory  
6     located at the memory address to aid in image processing tasks.
- 1           2.     The image signal processor of claim 1, further comprising a shared  
2     memory coupled to the plurality of the memory address generators, the shared memory  
3     storing data to be sent to the local memory and commands to be performed by the  
4     memory address generators.
- 1           3.     The image signal processor of claim 2, wherein the shared memory  
2     comprises a plurality of cluster communication registers.
- 1           4.     The image signal processor of claim 3, further comprising a cluster  
2     communication register interface to couple the plurality of cluster communication  
3     registers to the plurality of memory address generators.
- 1           5.     The image signal processor of claim 3, wherein the plurality of cluster  
2     communication registers include data cluster communication registers to store data and  
3     command cluster communication registers to store commands.
- 1           6.     The image signal processor of claim 5, wherein a pair of cluster  
2     communication registers are assigned to each memory address generator.
- 1           7.     The image signal processor of claim 6, wherein each pair of cluster  
2     communication registers includes a data cluster communication register and a  
3     command cluster communication register.
- 1           8.     The image signal processor of claim 3, further comprising an arbiter to  
2     arbitrate access to the local memory by the memory address generators.

1           9.     The image signal processor of claim 8, wherein the plurality of cluster  
2 communication registers are at least 16-bit registers.

1           10.    The image signal processor of claim 9, further comprising 16-bit data  
2 paths that couple the cluster communication registers to the memory address  
3 generators, the memory address generators to the arbiter, and the arbiter to the local  
4 memory.

1           11.    The image signal processor of claim 10, wherein the local memory  
2 includes static random access memory (SRAM).

1           12.    A method comprising:  
2 storing data in a local memory of an image signal processor;  
3 generating a memory address to the local memory utilizing a memory address  
4 generator within the image signal processor; and  
5 performing an operation on the data of the local memory located at the memory  
6 address utilizing the memory address generator to aid in image processing tasks.

1           13.    The method of claim 12, further comprising:  
2 storing data to be sent to the local memory in a shared memory of the image  
3 signal processor; and  
4 storing commands in the shared memory to be performed on the data in the  
5 local memory.

1           14.    The method of claim 13, wherein the shared memory comprises a  
2 plurality of cluster communication registers.

1           15.    The method of claim 14, wherein the plurality of cluster communication  
2 registers include data cluster communication registers to store data and command  
3 cluster communication registers to store commands.

1           16.    The method of claim 15, further comprising assigning a pair of cluster  
2 communication registers to one of a plurality of memory address generators, each  
3 memory address generator to generate a memory address to the local memory within

4 the image signal processor and to perform an operation on the data of the local memory  
5 located at the memory address to aid in image processing tasks.

1 17. The method of claim 16, further comprising arbitrating access to the  
2 local memory by the plurality of memory address generators.

1 18. The method of claim 14, wherein the plurality of cluster communication  
2 registers are at least 16-bit registers.

1 19. The image processor of claim 18, wherein 16-bit data paths couple the  
2 cluster communication registers to the memory address generators and the memory  
3 address generators to the local memory.

1 20. A machine-readable medium having stored thereon instructions, which  
2 when executed by a machine, cause the machine to perform the following operations  
3 comprising:

4 storing data in a local memory of an image signal processor;  
5 generating a memory address to the local memory utilizing a memory address  
6 generator within the image signal processor; and  
7 performing an operation on the data of the local memory located at the memory  
8 address utilizing the memory address generator to aid in image processing tasks.

1 21. The machine-readable medium of claim 20, further comprising:  
2 storing data to be sent to the local memory in a shared memory of the image  
3 signal processor; and  
4 storing commands in the shared memory to be performed on the data in the  
5 local memory.

1 22. The machine-readable medium of claim 21, wherein the shared memory  
2 comprises a plurality of cluster communication registers.

1 23. The machine-readable medium of claim 22, wherein the plurality of  
2 cluster communication registers include data cluster communication registers to store  
3 data and command cluster communication registers to store commands.

1           24.    The machine-readable medium of claim 23, further comprising  
2    assigning a pair of cluster communication registers to one of a plurality of memory  
3    address generators, each memory address generator to generate a memory address to  
4    the local memory within the image signal processor and to perform an operation on the  
5    data of the local memory located at the memory address to aid in image processing  
6    tasks.

1           25.    The machine-readable medium of claim 24, further comprising  
2    arbitrating access to the local memory by the plurality of memory address generators.

1           26.    The machine-readable medium of claim 22, wherein the plurality of  
2    cluster communication registers are at least 16-bit registers.

1           27.    The machine-readable medium of claim 26, wherein 16-bit data paths  
2    couple the cluster communication registers to the memory address generators and the  
3    memory address generators to the local memory.

1           28.    An image processor system comprising:  
2           a processor coupled to an image processor; and  
3           a double data rate synchronous dynamic random access memory (DDR  
4    SDRAM) coupled to the image processor, the image processor including a plurality of  
5    image signal processors coupled to one another, each image signal processor including:  
6           a local memory to store data, and  
7           a memory command handler including a plurality of memory address  
8           generators, each memory address generator to generate a memory address to the  
9           local memory and to interpret a command to be performed on the data of the  
10          local memory located at the memory address to aid in image processing tasks.

1           29.    The image processor system of claim 28, further comprising a shared  
2    memory coupled to the plurality of the memory address generators, the shared memory  
3    storing data to be sent to the local memory and commands to be performed by the  
4    memory address generators.

1           30.     The image processor system of claim 29, wherein the shared memory  
2 comprises a plurality of cluster communication registers.

1           31.     The image processor system of claim 30, further comprising a cluster  
2 communication register interface to couple the plurality of cluster communication  
3 registers to the plurality of memory address generators.

1           32.     The image processor system of claim 30, wherein the plurality of cluster  
2 communication registers include data cluster communication registers to store data and  
3 command cluster communication registers to store commands.

1           33.     The image processor system of claim 32, wherein a pair of cluster  
2 communication registers are assigned to each memory address generator.

1           34.     The image processor system of claim 33, wherein each pair of cluster  
2 communication registers includes a data cluster communication register and a  
3 command cluster communication register.

1           35.     The image processor system of claim 30, further comprising an arbiter to  
2 arbitrate access to the local memory by the memory address generators.

1           36.     The image processor system of claim 35, wherein the plurality of cluster  
2 communication registers are at least 16-bit registers.

1           37.     The image processor system of claim 36, further comprising 16-bit data  
2 paths that couple the cluster communication registers to the memory address  
3 generators, the memory address generators to the arbiter, and the arbiter to the local  
4 memory.

1           38.     The image processor system of claim 37, wherein the local memory  
2 includes static random access memory (SRAM).